

IGBT Chip

Die In Wafer Form

1200V
IC (nom) =75A
Vce(sat)typ=3.3V@IC(nom)@25°C
Fast IGBT
ShortCircuit Rated
150mm Wafer

Applications

- Welding Machine/ Cutting Machine
- Induction Heating/HF Power

Features

Non Punch Through (NPT) Technology
Low Etotol
10μs Short Circuit Capability
Square RBSOA
Positive Vce(sat) Temperature Coefficient

Chip Type	ICn	Vce	Die size	Wafer size
SYC75PN120WHF	75A	1200V	11.25*11.25 mm ²	6 inch

Mechanical Parameters

Die size	11.25mm*11.25mm
Emitter pad size	See chip drawing
Gate pad size	1.134mm*1.143mm
Active Area total	95.83mm ²
Silicon thickness	180um
Wafer size	150mm
Maximum possible chips per wafer	85pcs
Passivation frontside	Polyimide
Pad metal	4000nm AlSiCu
Backside metal	Al - Ti - Ni/V - Ag, (1kA - 1kA - 2kA - 8kA) suitable for epoxy and soft solder die bonding
Die bond	Soft solder
Wire bond	Al, ≤500um
Reject ink dot size	Ø 0.65mm; max. 1.2mm
Storage environment (<6 months) for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C
Storage environment (<6 months) for open MBB bags	Acc. IEC 62258-3; Section 9.4 Storage Environment.

Maximum Ratings

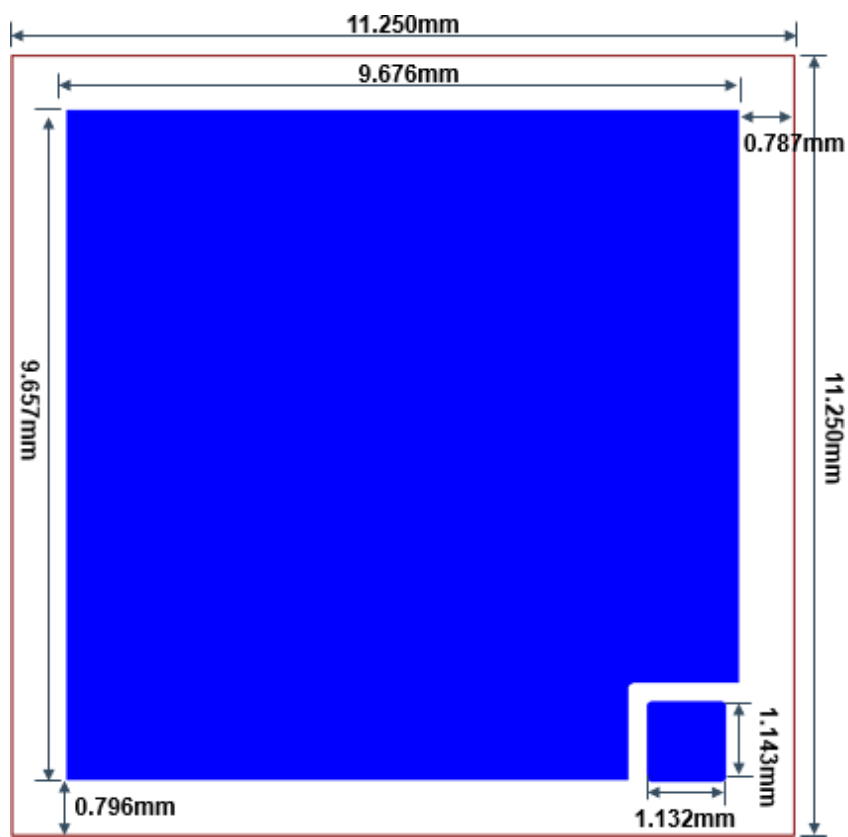
Parameter	Symbol	Value	Unit
Collector-emitter breakdown voltage, $T_{vj}=25^{\circ}\text{C}$	VCE	1200	V
DC collector current, limited by T_{vj} max 1	IC	75	A
Pulsed collector current, t_p limited by T_{vj} max 2	IC,puls	150	A
Gate-emitter voltage	VGE	± 20	V
Junction temperature	T_{vj}	150	$^{\circ}\text{C}$
Operating junction temperature	$T_{vj,op}$	-40 - 150	$^{\circ}\text{C}$
Short circuit data ^{2/3} $V_{GE}=15\text{V}$, $V_{CC}=600\text{V}$, $T_{vj}=150^{\circ}\text{C}$	tsc	10	μs

Static Characteristics (tested on chip)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	$V_{GE}=0\text{V}$, $I_C=250\mu\text{A}$	1200			V
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C=75\text{A}$, $V_{GE}=15\text{V}$, $T_{vj}=25^{\circ}\text{C}$	3.0	3.3	3.6	V
Gate-emitter threshold voltage	$V_{GE(th)}$	$V_{GE}=V_{CE}$, $I_C=1\text{mA}$, $T_{vj}=25^{\circ}\text{C}$	5.0	5.5	6.0	V
Collector-emitter leakage Current	I_{CES}	$V_{CE}=1200\text{V}$, $V_{GE}=0\text{V}$, $T_{vj}=25^{\circ}\text{C}$			20	μA
Gate-emitter leakage current	I_{GES}	$V_{CE}=0$, $V_{GE}=20\text{V}$, $T_{vj}=25^{\circ}\text{C}$			100	nA

说明：此规格书中的参数值是通过芯片CP数据评估制定，FT测试的时候同测试条件下 $V_{ce(sat)}$ 参数会降低（不同封装工艺可能也会不同），给出一个供参考的数值是在现CP规范上减少0.2V，以客户实际统计FT的bias为准。

1. Depending on thermal properties of assembly.
2. Not subject or production test - verified by design/characterization.
3. Allowed number of short circuits: <1000; time between short circuits: >1s.



Bare Die Product Specifics

Test coverage at wafer level cannot cover all application conditions. Therefore, it is recommended to test all characteristics which are relevant for the application at package level, including RBSOA and SCSOA.

Revision History

Revision	Subjects(major changes since last revision)	Date
1.0	Final date sheet	2019.12.25
1.1	Change specification name and company address	2022.10.27
1.2	Add ‘说明’	2023.3.22