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2 free download newest version from Kobo, the most popular e-book store with over 1 million titles. DOWNLOAD F.A.Q - Official site1. Field of the Invention The present invention relates to a method for fabricating a semiconductor device and, more particularly, to a method for fabricating a capacitor of a semiconductor device by means of self-alignment. 2. Description of the Related Art With high integration of DRAM devices, an area of a memory cell has decreased and a diameter of a capacitor has become fine. Thus, a method for increasing an effective area of a capacitor has been proposed. For example, a method for forming a capacitor having an increased effective area has been proposed wherein a storage electrode and a plate electrode are formed on a same layer with an insulating film therebetween and a contact hole for exposing a predetermined area of the storage electrode is formed in the insulating film and then the plate electrode is formed on the insulating film. In this case, a self-

alignment with respect to the contact hole is obtained by the method. FIGS. 1A to 1F are cross-sectional views for explaining a conventional method for forming a capacitor. As shown in FIG. 1A, a field oxide layer is formed on a semiconductor substrate 11 to define an active region. A channel stop ion is implanted into the semiconductor substrate 11 to form an n.sup.+ source region 12 and a drain region 13. A first interlayer insulating film 21 is formed on the substrate 11 to cover the field oxide layer and gate electrodes 14. A predetermined portion of the first interlayer insulating film 21 is removed by a well-known photolithographic technique and a gate electrode opening is formed. A conductive layer 22 is deposited on the first interlayer insulating film 21 and the gate electrode 14. A photoresist pattern 23 is formed on the conductive layer 22. By using the photoresist pattern 23 as a mask, the conductive layer 22 is etched to form a capacitor electrode pattern 24 and a bit line contact pattern 25. As shown in FIG. 1B, a second interlayer insulating film 26 is formed on the substrate 11 to cover the capacitor electrode pattern 24, the bit line contact pattern 25 and the first interlayer insulating film 21. The second interlayer insulating film 26 is planarized until the bit line contact pattern 25 is exposed by a well-known photolithographic technique and etching
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