

FRD Chip

Die In Wafer Form

1700V
IF=150A
VF typ=2V@IF(150A)@25°C
150mm Wafer

Applications

- Industrial Motor Drive
- UPS
- Welding
- Solar Inverter

Features

- Reduced Power Loss In Diode And Switching Transistor
- High Frequency Operation
- Optimized for switching softness, Reduced EMI

Chip Type	IF	VR	Die size	Wafer size
SYF150P170E1	150A	1700V	10.9*7.2 mm ²	6 inch

Mechanical Parameters

Die size	10.9*7.2 mm ²
Anode pad size	9.7*6.0 mm ²
Silicon thickness	250um
Wafer size	150mm
Maximum possible chips per wafer	158pcs
Passivation frontside	polyimide
Pad metal	4000nm AlSiCu
Backside metal	Ti - Ni - Ag suitable for epoxy and soft solder die bonding
Die bond	electrically conductive glue or solder
Wire bond	Al, ≤500um
Reject ink dot size	Ø 0.65mm; max. 1.2mm
Storage environment (<6 months) for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C
Storage environment (<6 months) for open MBB bags	Store in original container, in dry nitrogen, <6 months at an ambient temperature of 23°C

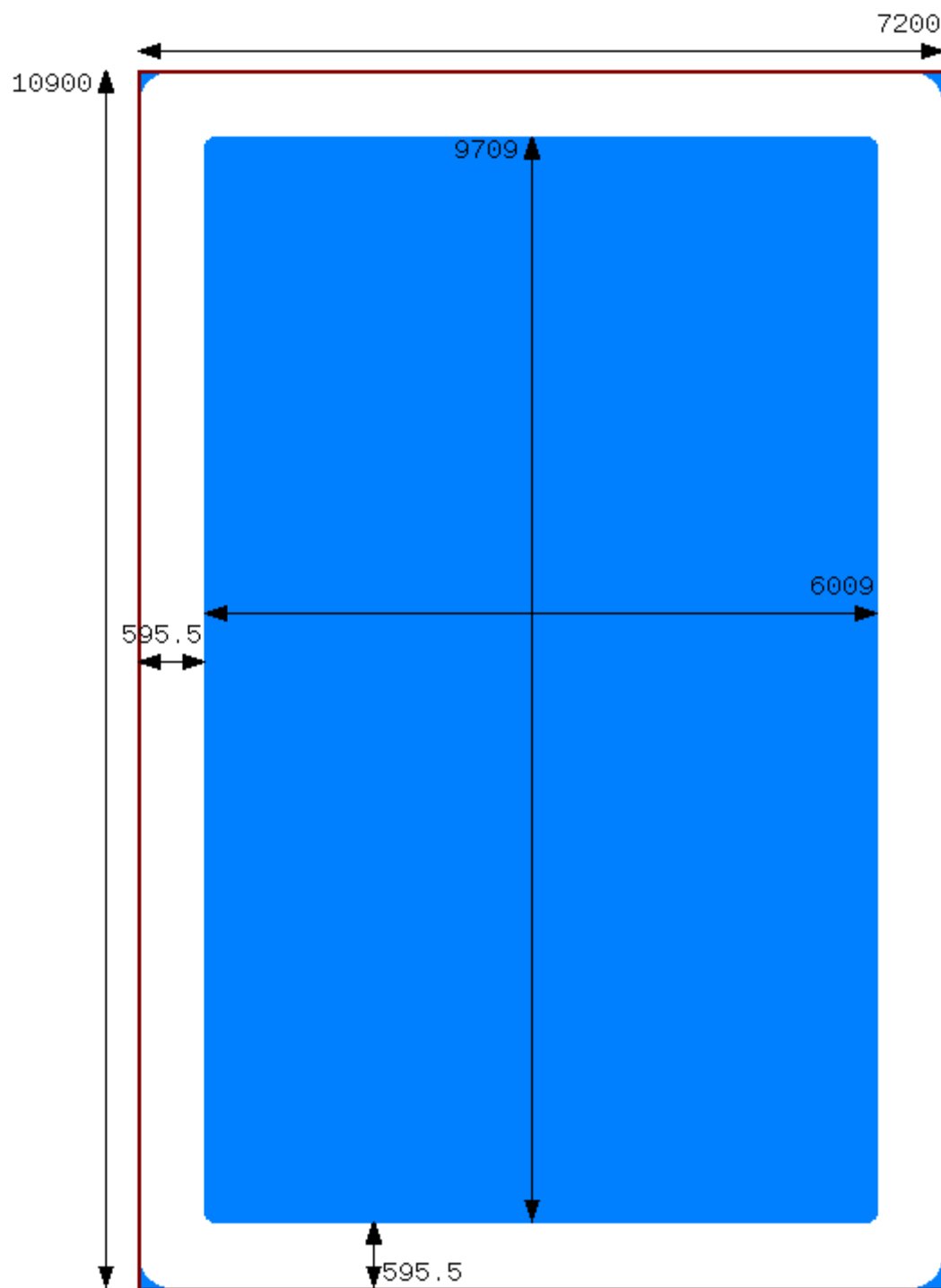
Maximum Ratings

Parameter	Symbol	Value	Unit
Minimum reverse breakdown voltage, $T_j=25^{\circ}\text{C}$	V_{RRM}	1700	V
Maximum continue forward current, $T_j=150^{\circ}\text{C}$	I_{FM}	300	A
Maximum reverse leakage current, $T_j=25^{\circ}\text{C}$	I_{RM}	20	μA
Maximum forward voltage, $I_F=150\text{A}$, $T_j=25^{\circ}\text{C}$	V_{FM}	2.0	V
Operating junction temperature range	T_j	$-55\sim+150$	$^{\circ}\text{C}$

Electrical Characteristics (tested on chip)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Breakdown voltage	V_{BR}	$I_R=200\mu\text{A}$	1700			
Forward voltage	V_F	$T_j=25^{\circ}\text{C}$, $I_F=150\text{A}$	-	2	-	V
Reverse leakage current	I_R	$V_R=1700\text{V}$, $T_j=25^{\circ}\text{C}$			20	μA

1. Depending on thermal properties of assembly.
2. Not subject or production test - verified by design/characterization.



Not to Scale(unit:um)

Notes:

1. Controlling dimension: millimeters
2. Die width and length tolerance:<0.05

Bare Die Product Specifics

Test coverage at wafer level cannot cover all application conditions. Therefore it is recommended to test all characteristics which are relevant for the application at package level, including RBSOA and SCSOA.

Revision History

Revision	Subjects(major changes since last revision)	Date
1.0	Preliminary date sheet	2024.1.10