IGBT Chip

Die In Wafer Form

1200V
IC (nom) =75A
Vce(sat)typ=2.5V@IC(nom)@25℃
Low Eoff
ShortCircuit Rated
200mm Wafer

Applications

- Welding
- Induction Heating
- High Frequency Power
- UPS

Features

Trench FS Technology

Low Eoff

10μs Short Circuit Capability

Positive Vce(sat) Temperature Coefficient

Chip Type	Icn	Vce	Die size	Wafer size
SYC75P120G4WF1	75A	1200V	7.80*9.00 mm^2	8 inch

Mechanical Parameters

Die size	7.80mm*9.00mm
Emitter pad size	See chip drawing
Gate pad size	1.37mm*1.3mm
Silicon thickness	120um
Wafer size	200mm
Maximum possible chips per wafer	316 pcs
Passivation frontside	Polyimide
Pad metal	4000nm AlSiCu
Backside metal	Al - Ti - Ni/V - Ag, (1kA - 1kA - 2kA - 8kA) suitable for epoxy and soft solder die bonding
Die bond	Soft solder
Wire bond	Al, ≤500um
Reject ink dot size	⌀ 0.65mm; max. 1.2mm
Storage environment (<6 months) for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C
Storage environment (<6 months) for open MBB bags	Acc. IEC 62258-3; Section 9.4 Storage Environment.

Maximum Ratings

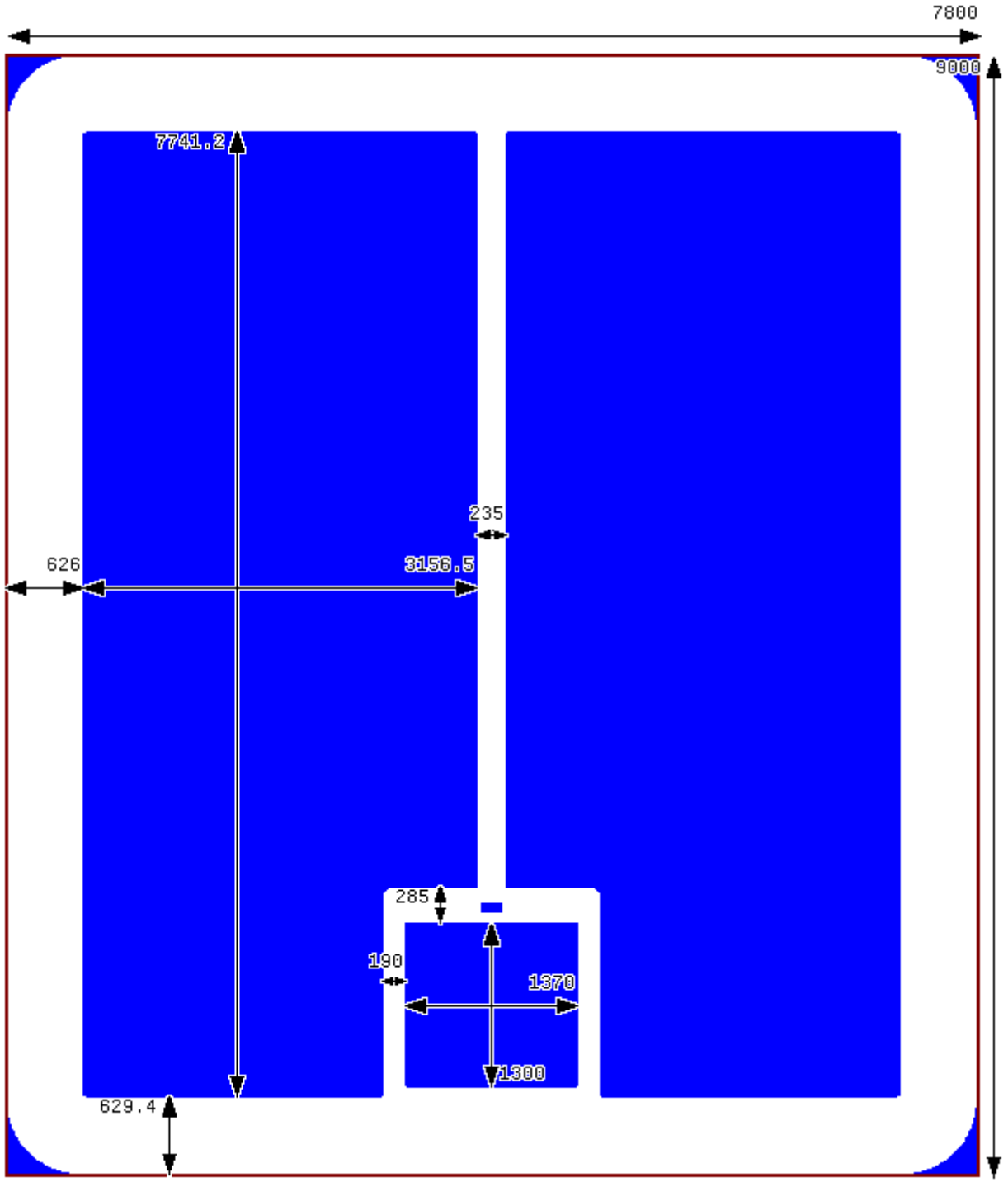
Parameter	Symbol	Value	Unit
Collector-emitter voltage, Tvj=25° C	VCE	1200	V
DC collector current, limited by Tvj max [1]	IC	75	A
Pulsed collector current, tp limited by Tvj max [2]	IC,puls	150	A
Gate-emitter voltage	VGE	±20	V
Junction temperature	Tvj	150	℃
Operating junction temperature	Tvj op	-40 - 150	℃
Short circuit data [2/3] VGE=15V, VCC=600V, Tvj=150°C	tsc	10	μs

Static Characteristics (tested on chip)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	V_{GE}=0V, I_C=250uA	1200			V
Collector-emitter saturation voltage	$V_{CE(sat)}$	Ic=75A,V_{GE}=15V, T_{vj}=25℃		2.5		V
Gate-emitter threshold voltage	$V_{GE(th)}$	V_{GE}=V_{CE}, I_C =1.5mA, T_{vj}=25℃		5.8		V
Collector-emitter cut-off current	I_{CES}	V_{CE}=1200V,V_{GE}=0V, T_{vj}=25℃			20	uA
Gate-emitter leakage current	I_{GES}	V_{CE}=0, V_{GE}=20V, T_{vj}=25℃			100	nA
Internal gate resistor	R_{gint}	Tvj=25℃		1		Ω

说明：此规格书中的参数值是通过芯片CP数据评估制定，FT测试的时候同测试条件下Vce(sat)参数会降低（不同封装工艺可能也会不同），给出一个供参考的数值是在现CP规范上减少0.2V，以客户实际统计FT的bias为准。

1. Depending on thermal properties of assembly.
2. Not subject or production test - verified by design/characterization.
3. Allowed number of short circuits: <1000; time between short circuits: >1s.


7800
9000
7741.2
235
626
3156.5
285
190
1370
1300
629.4

Bare Die Product Specifics

Test coverage at wafer level cannot cover all application conditions. Therefore, it is recommended to test all characteristics which are relevant for the application at package level, including RBSOA and SCSOA.

Revision History

Revision	Subjects(major changes since last revision)	Date
1.0	Preliminary date sheet	2023.3.24
1.1	Change name from GT75P120G4WF to GT75P120G4WF1 Change $V_{CE(sat)}$ from 2.6 to 2.5 Add parameter Rg	2023.10.25