IGBT Chip

Die In Wafer Form

1200V
IC(nom) =50A
Vce(sat)typ=2.4V@ IC(nom)@25℃
Low Vce(sat)
ShortCircuit Rated
200mm Wafer

Applications

- Inverter For Motor Driver
- BMS
- EV charger

Features

Trench FS Technology
Low Eswitch
10μs Short Circuit Capability
Parallel Suitable
Positive Vce(sat) Temperature Coefficient

Chip Type	Icn	Vce	Die size	Wafer size
SYC50P120H4WF	50A	1200V	6.37*6.5 mm^2	8 inch

Mechanical Parameters

Die size	6.37mm*6.5mm
Emitter pad size	See chip drawing
Gate pad size	1.22mm*0.84mm
Area total	41.4mm^2
Silicon thickness	130um
Wafer size	200mm
Maximum possible chips per wafer	562 pcs
Passivation frontside	Polyimide
Pad metal	4000nm AlSiCu
Backside metal	Al - Ti - Ni/V - Ag, (1kA - 1kA - 2kA - 8kA) suitable for epoxy and soft solder die bonding
Die bond	Soft solder
Wire bond	Al, ≤500um
Reject ink dot size	∅ 0.65mm; max. 1.2mm
Storage environment (<6 months) for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C
Storage environment (<6 months) for open MBB bags	Acc. IEC 62258-3; Section 9.4 Storage Environment.

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage, Tvj=25°C	VCE	1200	V
DC collector current, limited by Tvj max [1]	IC	50	A
Pulsed collector current, tp limited by Tvj max [2]	IC,puls	100	A
Gate-emitter voltage	VGE	±20	V
Junction temperature	Tvj	150	℃
Operating junction temperature	Tvj op	-40 - 150	℃
Short circuit data [2/3] VGE=15V, VCC=600V, Tvj=150°C	tsc	10	μs

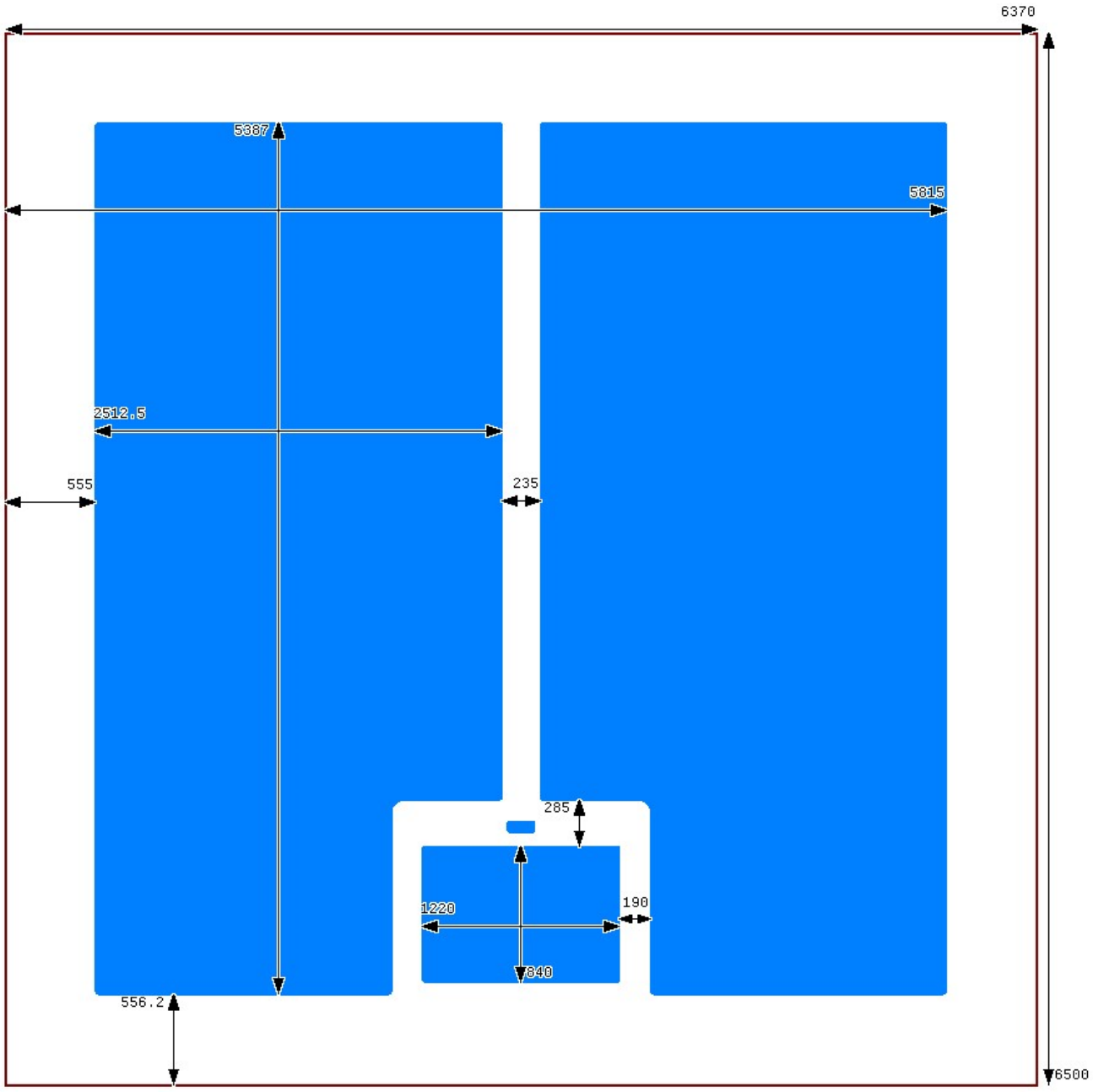
Static Characteristics (tested on chip)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	V_{GE}=0V, I_C=250uA	1200			V
Collector-emitter saturation voltage	$V_{CE(sat)}$	Ic=50A,V_{GE}=15V, T_{vj}=25℃	-	2.4	-	V
Gate-emitter threshold voltage	$V_{GE(th)}$	V_{GE}=V_{CE}, I_C =1mA, T_{vj}=25℃	-	5.7	-	V
Collector-emitter cut-off current	I_{CES}	V_{CE}=1200V,V_{GE}=0V, T_{vj}=25℃			20	uA
Gate-emitter leakage current	I_{GES}	V_{CE}=0, V_{GE}=20V, T_{vj}=25℃			100	nA
Internal gate resistor	R_{gint}	Tvj=25℃		1		Ω

说明：此规格书中的参数值是通过芯片CP数据评估制定，FT测试的时候同测试条件下Vce(sat)参数会降低（不同封装工艺可能也会不同），给出一个供参考的数值是在现CP规范上减少0.2V，以客户实际统计FT的bias为准。

此规格书中的芯片有效颗数以实际数量为准。

1. Depending on thermal properties of assembly.
2. Not subject or production test - verified by design/characterization.
3. Allowed number of short circuits: <1000; time between short circuits: >1s.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