

IGBT Chip

Die In Wafer Form

1200V
IC (nom) =150A
Vce(sat)typ=2.55V@IC(nom)@25°C
Low Eoff
ShortCircuit Rated
300mm Wafer

Applications

- Welding
- Induction Heating
- High Frequency Power

Features

Trench FS Technology

Low Eoff

10μs Short Circuit Capability

Positive Vce(sat) Temperature Coefficient

Chip Type	Icn	Vce	Die size	Wafer size
SYC150P120C4WF	150A	1200V	11.40*12.36 mm ²	12 inch

Mechanical Parameters

Die size	11.40mm*12.36mm
Emitter pad size	See chip drawing
Gate pad size	1.32mm*1.32mm
Area total	139.21mm ²
Silicon thickness	120um
Wafer size	300mm
Maximum possible chips per wafer	410 pcs
Passivation frontside	Polyimide
Pad metal	5000nm AlCu
Backside metal	Al - Ti - Ni/V - Ag, (2kA - 2kA - 2kA - 8kA) suitable for epoxy and soft solder die bonding
Die bond	Soft solder
Wire bond	Al, ≤500um
Reject ink dot size	ø 0.65mm; max. 1.2mm
Storage environment (<6 months) for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C
Storage environment (<6 months) for open MBB bags	Acc. IEC 62258-3; Section 9.4 Storage Environment.

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage, $T_{vj}=25^{\circ}\text{C}$	VCE	1200	V
DC collector current, limited by T_{vj} max ¹	IC	150	A
Pulsed collector current, tp limited by T_{vj} max ²	IC,puls	300	A
Gate-emitter voltage	VGE	± 20	V
Junction temperature	T_{vj}	150	$^{\circ}\text{C}$
Operating junction temperature	$T_{vj\text{ op}}$	-40 - 150	$^{\circ}\text{C}$
Short circuit data ^{2/3} $V_{GE}=15\text{V}$, $V_{CC}=600\text{V}$, $T_{vj}=150^{\circ}\text{C}$	tsc	10	μs

Static Characteristics (tested on chip)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	$V_{GE}=0\text{V}$, $I_C=250\mu\text{A}$	1200			V
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C=150\text{A}$, $V_{GE}=15\text{V}$, $T_{vj}=25^{\circ}\text{C}$		2.55		V
Gate-emitter threshold voltage	$V_{GE(th)}$	$V_{GE}=V_{CE}$, $I_C=1.5\text{mA}$, $T_{vj}=25^{\circ}\text{C}$		5.8		V
Collector-emitter cut-off current	I_{CES}	$V_{CE}=1200\text{V}$, $V_{GE}=0\text{V}$, $T_{vj}=25^{\circ}\text{C}$			20	μA
Gate-emitter leakage current	I_{GES}	$V_{CE}=0$, $V_{GE}=20\text{V}$, $T_{vj}=25^{\circ}\text{C}$			100	nA
Internal gate resistor	R_{gint}	$T_{vj}=25^{\circ}\text{C}$		0		Ω

说明：此规格书中的参数值是通过芯片CP数据评估制定，FT测试的时候同测试条件下 $V_{ce(sat)}$ 参数会降低（不同封装工艺可能也会不同），给出一个供参考的数值是在现CP规范上减少0.2V，以客户实际统计FT的bias为准。

此规格书中的芯片有效颗数以实际数量为准。

1. Depending on thermal properties of assembly.
2. Not subject or production test - verified by design/characterization.
3. Allowed number of short circuits: <1000; time between short circuits: >1s.

