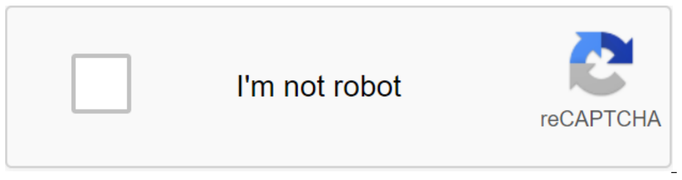

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Cadence virtuoso tutorial pdf

Welcome to Virtuoso, a full custom layout editor from Cadence, Inc. Virtuoso is more than just a layout editor. It's a full layout environment. Interactive View and Editing hierarchical layout Hierarchical and gradual DRC Built into netlisting Interactive Communication Tracking Interactive Tool Wiring Interfaces to Other Tools, including schematic capture (e.g. Analog Artist), as well as the DRC and LVS package (e.g. Caliber) Smart Palette for easy control and feedback on layers Full customization and extension through Tcl/Tk script language and independence API technology using file descriptions of technologies optimized for large databases Very Fast Redisplay for all Chip View and Inspection reads/writes GDSII works on Solaris. This tutorial is based on the North Carolina State University Cadence Design Kit (NCSU CDK). The tutorial will introduce you to some features. For more information, contact the Virtuoso Guide and online documentation. From the icfb window, bring up the library manager from the tool menu (choose the tools/library manager) In the library manager, create a new library called ee141_lab2 (choose file/new/library). This will open a new dialogue window in which you need to enter the name of your library, the library path and attach to the existing technical library (TSMC 0.24u must be selected). After filling it all up, the window should look something like this: Click the Good Create a NanD cell view layout. Just in a nand2 called a cell and a mock-up masquerading. Hit Enter, the next window will appear: Select Virtuoso tool, View Name is automatically installed on the layout Once you hit OK, the virtuoso screen will appear as shown below (besides, the LSW box with different layers of mask will automatically pop up): In this window, you place the transistors, draw mask layers, etc. at the top of the window the head bar should say: ee141_lab2 Virtuoso This means that you are editing a nand2 cell layout view from ee141_lab2 library. Next, on top you should see the bar menu, which contains the following menu items: Tools, Design, Window, Create, Edit, Check, Link, Options, Route and Skills. This is a retractable menu just like any PC or Mac app. At the bottom of the window is the area of virtuoso messages. It is activated when there is some work that describes the task being done. He can say something like a select figure that will be stretched..... The Virtuoso Message Area is a kind of mini-assistance feature. The LSW window is an intelligent palette. The smart palette provides many features. o It controls which layers are visible and allows you to select layers for painting. o He gives feedback on what's in time is under the cursor, and that is currently chosen. o This allows you to control what layers may be A description of the different layers of the mask can be found here. Before we go any further, here's how to get help if you ever need it. There are several levels of help available online for Virtuoso users. You already know about the quick help listed in the field of virtuoso messages. In addition, you can access a full online guide, a full list of active hot keys and full text team documentation at any time. Before you go on you have to bring up the Virtuoso Guide and see what's out there. The guide is a reference to V.irtuoso and contains a lot of information that you won't find in this simple tutorial. Okay, let's start on some layout. Go to the Virtuoso window and hit i (instant)... This will lead to the following window, click on the Review and select NCSU_Tech_Lib_03d: Next, select nmos from the NCSU_TechLib, the choice should look like this: Click Close and then go back to the previous window and click Hide, place the cursor in the Virtuoso window where you want your nmos posted. Now you'll notice that Virtusoso works with a grid that is very rough by default. Also, you won't immediately see what's inside the nmos symbol. Let's fix this: from the Virtuoso Options menu, select the display and set display levels from 0 to 10, as well as the X and Y Snap Spacing up to 0.06 (it's 0.06 half lambda, lambda is 0.12 in this 0.24um technology). The display settings should be as follows: Click Save and then OK. Now you can see the layers of the mask in nmos, you will later realize that you will be able to place your components on the grid with much finer precision, the accuracy of the semi-lambda (0.06). Your nmos transistor probably looks very small on the screen, hit z (zoom) and then hold the left mouse button to select the area you want to enlarge. The enlarged nmos should look like this: Please note that only the active layer is used, and this is normal. (There is no p-good because it is a p-substrate process.) Learn more about macro layouts such as nmos here. Now, edit the properties of the instance, click on nmos, when the transistor is high in content, click q. Click on The Settings and change the width to 1.98u (2.0u will be automatically changed to 1.98u due to geometric interval rules). Since we eventually want to use this device to make 2 NAND input gates, change your fingers to 2. Now click OK. Two nfet combined (stacked) together should appear. Type f (hot key for all - zoom to fit under the window menu) and the layout should appear in the center of the window. Now the screen should look like this: TIP! You can undo everything you just did at Virtuoso. Use the hot u key or select Cancel from the Edit menu. You can also redo what you have just Shift-u hotkey. Now zoom in by typing shift-z, or zoom in on the window menu. There are several scaling methods found in the View menu. One easy way to zoom up to the exact region you want is by using the zoom hot key. This brings you into zoom mode. Please note that the cursor has changed. Then hold the left button (Button-1) and drag the box that surrounds the area you want to enlarge. When you release your mouse, the screen will grow to where your box is. If you mess up, don't panic. Remember that F will always zoom in to match. Hotkey shift-z can be used to scale twice. When Virtuoso is in basic mode (by default), if you simply drag the area by holding the left button (Button-1), everything in the box will be selected when the button is issued and highlighted in white. Drag the box over the folded nfet's we just drew. When you release the mouse button, everything that is selected, in this case the fet cell, will be highlighted. Once you have chosen an object or paint you can do a lot of things with it. For example, you can move it by entering the hot key. You can move the layout up/down/left/right one grid at a time by clicking on the selection and moving the mouse. Give it a shot. You can also choose objects or paints by clicking on them. Clicking on the left mouse button once on a piece of paint selects that particular rectangle of paint. Clicking once on a landfill or cell will select an object. Virtuoso supports Cut, Copy, and Paste in the same format as you'll see on any good Mac or PC-based drawing or drawing program. Council! All the scaling, moving, cutting and inserting, rotation, etc. functions that we've just performed with hot keys also have menu equivalents that can be found on the Edit menu. Select Verify/DRC to perform a design rule check (DRC). The FORM of DRC appears: Click OK to run THE DRC. Now add a 4 micron-wide pmos transistor and a 2-point multiplier. Place it close to nmos as shown below: Choose Check - DRC and Hit OK. Chances are you'll see some DRC errors. View BUGS DRC Use check - marker - Explain to see more information about flagged errors. Errors are described in the token text window as this one. In this particular case, the active Source/Drain was too close to the edge of n-well. You need a minimum required distance of 0.7 cm. Fix this error by moving pmos. Esc cancels the explanation command, the marker text window will disappear. To remove error flags, select Verify - Marker - Delete All Hit OK to remove all error flags. Now we are going to paint a piece of poly to connect the pfet and left the nfet gate together. Choose a poly layer Palette, hit the g draw rectangle and draw the poly area. Your layout should look like this: Use r and p hotkeys to draw rectangles and paths, wire up to two left contact regions and add a connection to the right Contacts. If you're having trouble with command p, see the following section for some hints. Consult CDK guides if you need to. Your layout should look like this (practical tips: periodically run a DRC check to make sure you're making progress in the right direction): Type F2, or choose Save from menu design (also a good thing to do from time to time). Let's say we're laying out this NAND gate for a standard cell library. Also, suppose that the power and ground rails work in metal 1 (M1) and that they are 2.04um wide (2.0um will not work due to mesh detail, which is 0.06um...). To add power to the M1 and ground wires: 1) Install metal1 as an active layer in the LSW window. 2) Type p bring up Create a Path menu. 3) Set Width to 2.04. 4) Draw a path where you want to place the Vdd. You can always choose again the path you have drawn and enter q to change its properties. Council! You can change the path size or rectangle by stretching the edge with the Stretch command found in the Edit menu. It's just that The Cursor is changing so you know you're in Edit Edge mode. Now move your finger over the edge that you want to stretch. The line will show you which edge you are more. If you have an edge you want to press the left mouse button (Button-1) and move the mouse in the direction you want to stretch the edge. (Note that you can only change the length along the way - to use the width of q and the property menu). Once you have drawn the top power line you can simply copy it and move it down. Now that you have laid out your power and ground rails you have to wire them using the wiring mode as before. Your cell should look like this: Please note that the entrances and exits are in power belts. What if they need to be brought in so the router can get to them? Let's say the router requires all the signals to be at the top of the cell and in the M1. You need to route the poly wires along the M1 power belts and then change to the M1. Virtuoso can make this work easier, as it can insert all the contacts needed to go from one layer to another. For example, if you need to go from poly to M1, then you just start drawing a path (p type) into a poly, and then press the left mouse button somewhere near where you want the contact to be and change the layer in the menu to create a path on metal1. What you see is that the tip of the wire turns into a contact that you can place. Now you can continue to draw your way in a new layer. Using the P command, extend both poly lines over the Vdd strap and complete their M1. Your layout should now look like this (run the DRC to make sure it's DRC-clean!): We get to get to finish this cell and your boss has just informed you that the power rails have been changed from the M1 to the M2. To change them, simply select the top (Vdd) rail and hit q to enter the layer properties. Change the layer to metal2, as shown below, and press OK. Repeat this for the lower (Gnd) rail. Now go ahead and attach power lines and ground lines to the new M2 straps. Just use the path mode to do this. Start with the M1 wires. When you are over the M2 straps click the left mouse button and change the layer to metal2. The next route is output to the top above the M2 near the entrances so the router can get to it as well. Your layout now has to look like this: There is one last thing before we finished with our NAND gates. It would be very useful to add pins with text labels on our layout. To add a text-tag pin, simply select Pin... From the Create menu. Click next to the contact form to open the form to create a Pin-shape: In the form of Create Shape Pin, bring the following in the box Terminal Names: vdd! Gnd! from In1 In2 Tap Pin Name Display to link the name to the pin. 1) Create a rectangle for vdd! The pin coincides with the power line at the top of the NAND. (start the vdd! pin in the bottom left corner and finish vdd! pin in the top right corner). 2) Name vdd! appears next to the cursor after pressing the second corner (top right corner). 3) Move the cursor to the vdd seat! text in the right place and then click to place the contact name there. 4) If the text looks too big, you can choose it, in a swirl q, to bring the window properties and edit its height. Continue the steps 1-3 above to create other contacts in the specified sequence (vdd! gnd! from in1 in2). Once you're done, your layout should look like this: Our little example of the NAND gate now has to be done. Big projects and hierarchies Now let's use our NAND gate and inverter (which you need to create. tip: just change the NAND...) cell to build something a little bigger. As a library manager, create a new cell called Row Now you have to edit the view of the cell layout of the row. Instant NAND four times and an inverter once to form an array of cascading cells. Your layout will look like a bit of a figure above if you are chosen to view all the inner layers. Now you can see what is inside the NAND2 cells and the inverter. To do this, hit hotkey e and set display levels from 0 to 10, for example. This will show all the layers inside the cells, as shown below: OK, now that we are here, say, our boss comes again and says: Sorry, but you have to bring outputs to the bottom of the cells. First, select the INV cell using and hit hotkey x (for design - Hierarchy - Edit on the spot). wire to bring outes to the bottom of the cell. Save the cell and type B (capital!) to get back up. Do the same for

the NAND cell (note that all four instances will be updated - this is expected since you changed the NAND cell from your library. Your layout should look like this: Now, just for a smirk, let's wire up to two gates. Since we want to wire them up in a row and not in NAND or inverter, we must first make sure the row is our editing cell. Now that the line is your cell editing, just use the posting strategy you learned in this tutorial to connect a couple of wires. The image below shows the zoomed in field of view to show two gates wired within the line cell. To learn more about Virtuoso and Analog Artist (Schematic Editor) Use openbook for Cadence tool documentation. And as always, the best way to really learn the program is to use it! This is! cadence virtuoso tutorial for beginners. cadence virtuoso tutorial layout. cadence virtuoso tutorial youtube. cadence virtuoso layout xl tutorial. cadence virtuoso simulation tutorial. cadence virtuoso digital implementation tutorial. cadence virtuoso inverter tutorial. cadence virtuoso ade xl tutorial