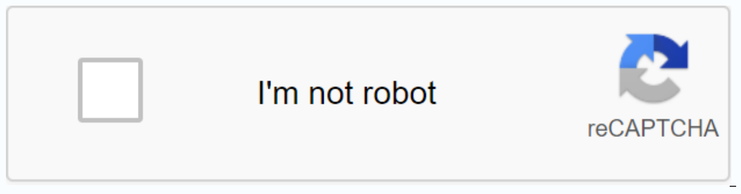
Advanced digital design with the ver



Continue

Area: Elec Eng School, Comp and Mathematics Sci (EECMS) Credits: 25.0 Contact Hours: 5.0 LESSON PATTERNS: The course model provides detailed information about the types and durations of classes. This will only be used as a guide. Precise information is included in the unit outline. Lesson: 1 x 2 Hours Weekly Computer Lab: 1 x 3 Hours Weekly Equivalent(s): 308791 (v.2) Advanced Digital Design 320 or any previous version Anti Required(s): 11338 (v.3) Computer Aided Engineering Digital Systems 601 or earlier AND CMPE6 60001 (v.1) Computer Aided Engineering of Digital Systems or previous version Prerequisial(s): 308768 (v.1) Basics of Digital Design 201 or earlier OR CMPE2001 (v.1) Basics of Digital Design or previous version ONE REFERENCES, TEXTS, RESULTS AND UPDATE DETAILS: The most up-to-date information about unit references, texts and results will be provided in the unit outline. Curriculum: Under Digital Abstraction. Field Programmable Logic Devices. Use VHDL (VLSL hardware design language) to define custom IP. Design of embedded systems of FPGA (field programmable gate array). Universal Design Methodology (UDM). Synthesis and verification. Design for Testing (DFT). Timing analysis. Introduction to common design. Design with kernels. Training Area: 031305 Computer Engineering Result Type: Grade/Sign Year Lifetime Built-in Part Online Full Online 2021 Bentley Perth Campus Semester 1 Y 2021 Miri Sarawak Campus Semester 1 Y 2021 Sri Lanka Inst Info Tech Semester 1 Y Partially Online Built-in means some (some) learning provided by interacting with or downloading prepackaged material from the Internet but regular and continuous participation with a face-to-face component is maintained. The Center for External Full Online remains working through the Curtin Bentley-based Distance Learning Area, partly excluding online internal courses/units (which means the main (large part) mode of learning provided through Internet interaction (including downloading prepackaged material on the Internet). The online courses/units running in the Curtin Bentley-based Distance Education Area, which remains Central External Information in this publication, are accurate and subject to change during printing. In particular, the University reserve the right to change the content and/or method of evaluation, change or change

tuition fees for any work unit, withdraw any training or program it offers, impose limitations on enrollment in any unit or program, and/or change regulations for any program. It does not claim that the material constitutes legal or professional advice. Curtin accepts no clear or unedied responsibility for accuracy or reliability in any matter, and It's on the air. Curtin University is not responsible for the results of any trust that may be put into this material by any person, except where otherwise required by legislation. Curtin will not be responsible to you or any other person for any loss or damage (including direct, consequence, or economic loss or damage) arising directly or indirectly from the use of this publication. International students studying on student visas in Australia can only study full-time, and there are also special entry requirements that must be met. Some of the information contained in this publication may not apply to international students, see international.curtin.edu.au information. Australian citizens, permanent residents and international students studying outside Australia may have the option of full-time, part-time and external education, depending on course availability and domestic requirements. Trainer: Gabe Cohn Office: CSE 507 Email: gabecohn (AT) uw [d0t] edu Office Hours: Friday 1.30pm-2.30pm CSE 507, or appointment TA: Edward Wang Office: CSE 507 Email: ejaywang (AT) uw [d0t] edu Office Hours: Tuesday 10:00-11:00 CSE 003, or appointment Course E-mail List: CSE467a_Au13 (AT) uw [d0t] edu Course and Laboratory Time Course: MWF 9:30-10:20 Location: CSE 303 Lab Part: Th 9:00-11:50 Location: CSE 003 Course Description CSE 467 Advanced Digital Design (4): Advanced techniques in the design of digital systems. Hardware description languages, combination and sequentual logic synthesis and optimization methods, partitioning, mapping to regular structures. Emphasis on reconfigurable logic as an application tool. Memory system design. Digital communication with serial/parallel and synchronous/concurrent methods. Prerequisite: CSE 352 or CSE 370; either CSE 326 or CSE 332. Course Objectives To provide an in-depth understanding of digital systems and designs, from specification and simulation to construction and debugging. Students should learn how to build and optimize algorithms that will work very quickly on custom hardware. Textbook There is no good textbook for this course. We will use the following textbook as a reference from CSE 352. We cover many of the basic concepts we will be using and are an excellent treatment of design with Verilog. I strongly recommend reading the Verilog section and follow the style given there. Try to forget about other Verilog styles you might have learned by reading Verilog references that describe everything you can do with Verilog without telling you how to use Verilog. Title: Digital Design and Computer Architecture Authors: David Money Harris and Sarah L. Harris Publisher: Mogan-Kaufman 2007 Errata: Here Will Be A Few Assignments on Homework given for a quarter of a second. Homework will usually be given on Wednesdays and will be given at the beginning of the class the following Wednesday (unless otherwise stated). Assignments delivered more than 10 minutes late (after 9:40) will be subject to a 10% penalty. For each additional day (including weekend days) when the assignment is late, an additional 10% of the score is deducted. Assignment issues can sometimes be rated randomly. To get full credit for an assignment, of course, you need turn-in solutions for each assigned issue. Only a subset of problems can be rated in detail. You won't know in advance what issues this will be, so make sure you do it all. Please carefully review assignment solutions before querying a note with an instructor or lecturer. Labs Labs form an important part of the class. Laboratories will usually be given out on Mondays and will be due at the beginning of the class (unless otherwise specified) on the following Monday. Laboratories returned more than 10 minutes late (after 9:40 a.m.) will be subject to a 10% penalty. For each additional day (including weekend days) when the assignment is late, an additional 10% of the score is deducted. Much of the lab can be completed in the 3-hour lab section on Thursdays, but additional time will be required outside the laboratory section. The first two laboratories will be completed separately, but most of the remaining laboratories will be built in groups of two. Last Project The final project is an expanded laboratory that will last several weeks at the end of the course. All the labs are built on the latest project. Like most laboratories, the final project will be completed in twos. The exams will not be final exams, but will be a 50-minute intermediate exam. The student can use a single note sheet in the exam. Collaboration and Cheating It is well known that students can learn a lot from each other given the chance. I suggest you work with each other. However, I also expect homework, laboratories and design issues to be their own in the delivery business. In other words, even if you get ideas from other students, you're responsible for understanding the design to the point where you can put it together and run it. We also encourage you to help other students; However, while it's good to discuss ideas or help debug a design, please don't do their job for them. I expect you to have the job you surrendered to. To the extent that you receive help, you should appreciate it. When you make a common problem or lab, all names must be in the assignment. The grade will be roughly determined as: Homework: 13% Labs: 40% Intermediate Exam: 15% Final Project: 32% I do not grade on the curve. I'd appreciate it if everyone got 4.0. Portions of this site may be re-printed or adapted for non-profit academic purposes, resource is correctly quoted and credited. CSE 467 Website: Copyright 2013, Department of Computer Science and Engineering, University of Washington. Advanced Digital Design (WS 2019) The course focuses on advanced scheduling issues in digital design. The need for design methodologies is discussed in detail, and alternatives to the traditional synchronous design style include global asynchronous local synchronous (GALS) and fully asynchronous styles (limited delay and delay insensit desensitisation). The scope extends from basic theory to practical design flow. In the context of synchronous design and GALS, metasability issues are discussed in great detail. This course focuses on advanced scheduling in digital design. The need for design methodologies is discussed in detail, and alternatives to the traditional synchronous design style include global asynchronous local synchronous (GALS) and fully asynchronous styles (limited delay and delay insensit desensitisation). The scope extends from basic theory to practical design flow. In the context of synchronous design and GALS, metasability issues are discussed in great detail. The course includes a mix of course blocks, exercise blocks and laboratories. The last two homework assignments are about discussing (questions/calculations and circuit designs results, respectively). Labs are optional as an extra course (LU) that can be taken in addition to lessons/exercise (VU). The course can be done without taking the exercise lab, but vice versa. Course materials (course slides, assignments, auxiliary materials) can be downloaded from TUWEL. Solutions must be provided as .pdf and uploaded to TUWEL before 12:00 noon, the day before the relevant exercise block. Course Dates Please register for the TISS Entrance and Lectures Overview course : An overview of the courses offered by our group during the 19/20 winter period will be given at an entrance class in the Seminar hall on Tuesday, 19/20 at 9:15 pm. Regular Lessons and Exercises: The normal course date is Wednesday 10:00-12:00 seminar hall BA 02A. In addition, there are extra slots for presentation of assignments and (optional) laboratory exercises, i.e. see the table below the Final Exam for the detailed program in the seminar hall from 13:00 to 15:00 on selected Tuesdays: The final written exam is available at TUWEL on 29 January 2020 and ba 02A. Course Materials Course slides, assignments and additional materials are available in the seminar hall from 10:00 to 12:00. For courses on Asynchronous Logic Design, the following textbook is also recommended: Jens Sparso and Steve FurberPrinciples of Asynchronous Design -- A Systems PerspectiveKluwer Academic Publishers, 2001 For Chapter 1 - 7 free .pdf version of this book is available on jens sparso homepage. A very good survey on asynchronous logic can also be found in the following articles:S.M. Nowick, M. Singh, Asynchronous Design-Part 1: Overview and Latest Developments, IEEE Design & Test, vol 32(3) andS.M. Nowick, M. Singh, Asynchronous Design—Part 2: Systems and Methodologies, IEEE Design & Test, volume 32(3). A very good introduction and survey of static pipelines can be found in the project report of our clap students. More details about Asynchronous Pipelines survey article S.M. Nowick, M. Singh, High-Performance Asynchronous Pipelines: An Overview, IEEE Design & Test of Computers, vol 28(5), 2011 Comparison of lag-free codes and an effective method for building completion detectors can be found in conference documents originating from our students' projects. For additional reading about Synchronizers, the following book recommended David J. Kinniment and Alex Yakovlevsynchronization and Arbitration Digital SystemsWiley, as well as article Ran Ginosar, Metastabilty and Synchronizers: A Tutorial, IEEE Design & Test of Computers, vol 28 (5), 2011. Robert Kutschera's master's thesis provides extensive research on synchronised techniques. Program: Moon Date Daytime Subject 2 October 10:00 - 12:00 1 - Organization, Role of Time 9 Wed 10:00 - 12:00 2 - Timing Model & Synchronous Design 16 Wed 10:00 - 12:00 2 - Timing Model & Synchronous Design Tuesday, November 5 at 13:00 - 15:00 3 - Metastability Models 6 Wed 10:00 - 12:00 3 - Metastability, Senkron12 Tue 13:00 - 15:00 4 - Metasability Measurement, GALS Design 13 Wed 10:00 - 12:00 4 - GALS Design , Pausable Clocks 19 Tue 13:00 - 15:00 5 - Asynchronous Design - Principles, Data Together 20 Wed 10:00 - 12:00 RA - Discussion Exercise 1 26 Tue 13:00 - 15:00 DA - Discussion Design 1 27 Wed 10:00 - 12:00 6 - Delay Insensitive Asynchronous Design Styles December 4 Wed 10:00 - 12:00 6 - Delay Insensitive Insensitive Asynchro Nous Design Styles 10 A tue 13:00 - 15:00 7 - Asynchronous Data Flow Structures 11 Wed 10:00 - 12:00 00 RB - Discussion Exercise 2 17 Tue 1pm - 15:00 DB - Discussion Design 2 18 Wed 10:00 - 12:00 8 - Synthesis Control Circuits 8 January 10:00 - 12:00 9 - Description Methods for Asynchronous design 14 Tue 13:00 - 15:00 10 - Asynchronous EDA 15 Wed 10:00 - 12:00 RC - Discussion Exercise 3 2 1 Tue 1pm - 3pm DC - Discussion Design 3 22 Wed 10:00 - 12:00 11 - 50 Shades of Synchrony 29 Wed 10:00 - 12:00 Pm Written Exam Rating Course ratings for the following schema exercises (based on the quality of solutions offered , solution presentation): 40% written exam: 40% of the remaining 20% can be achieved through contributions to discussions during lectures and exercise discussions, at least 40% can be reached for a positive grade exams and exercises should be reached at least 50% in general; accordingly, the boundary lines for other classes will be 62.5%, 75%, 87.5%. The rating for the laboratory will be as: quality of solutions submitted: presentation of 75% of solutions: 25% Re-overall at least 50% should be achieved a positive rating; accordingly, the boundary lines for other classes will be 62.5%, 75%, 87.5%. The aim will be to pass on the following competes: understanding the theoretical basics of synchronous design style to deal with challenging (timing) issues of digital design (esp. clock domain migration) and selecting the appropriate style for a specific problem of alternatives The limitations of the subject understand the limitations of the metasability of the basic concept and synchronous design: reasons and effects, modeling, MTBU forecasting and measurement design, and different settings GALS-Systems (synchronised implementation for time-crossing, transition pausable clocking) internal design, Limitations of basic building blocks of function and asynchronous design: Muller C-Element and Mutual Exclusion Element asynchronous design methods (packaged data, delay insensitive), handshake principles (2-phase /4-phase) and timing models (packaged data, delay insensitive,...) synchronous and concurrent logic Lecturer Dipl.Ing-ing asynchronous design comparison basic explanation methods. Dr.techn. Steininger Andreas Home